Amendments to the Specification

Please replace the paragraph that begins at page 7, line 28 with the following:

The secondary stage amplifier 30 comprises an input bipolar transistor ET and an output bipolar transistor AT. The input terminal of the input bipolar transistor ET is connected to the RF input HFin. The emitter terminal of the input bipolar transistor ET is connected to a reference potential, in the shown embodiment ground, via a resistor Re1. The collector terminal of the output bipolar transistor AT is high frequency coupled to the RF output RFout, in the illustrated embodiment via a diode D1 and a decoupling ~~capacity~~ capacitor C1. Further, the collector terminal of the output bipolar transistor AT is connected to a supply voltage terminal 32 via the diode D1, across which a supply voltage is applied, which operates the diode D1 in flow direction and provides to the operating current for the output bipolar transistor AT. The diode is not necessarily required, but it is advantageous in such that it provides normally a lesser ~~capacity~~ capacitance to the main stage than the transistor AT.

Please replace the paragraph that begins at page 9, line 10 with the following:

First, it is assumed, that the main stage is active and the secondary stage is inactive. In this case, a potential of 0 volt is applied to the bias terminal Biasl in the shown embodiment. At the base terminal of the main stage transistor VT1, its operating point potential is applied, which is, for example, 0.8 volt. Thus, the collector base voltage of the input transistor ET is 0.8 volt, so that the base collected diode of the input

bipolar transistor ET is reverse-biased. Thus, the base collector diode shows the smallest possible ~~capacity~~ capacitance. The base ~~collected~~ collector diode of the output bipolar transistor AT is also reverse-polarized, since a predetermined positive potential of, for example, about 2.7 volt is present over Vcc at a circuit node 34, while the base terminal of the output transistor AT is 0 volt.

Please replace the paragraph that begins at page 9, line 25 with the following:

The diode D1 is provided to achieve that the main stage sees also at the output only a small capacity, in series with the base collector ~~capacity~~ capacitor of the output bipolar transistor AT. The diode D1 is biased in flow direction by the potential at the circuit node 34. Providing the diode is optional, to improve the performance at the output, since the output bipolar transistor, to achieve a predetermined amplification and to achieve a desired output matching, respectively, can be designed with regard to its size such that no desired decoupling can be achieved at the output in the reverse direction by its collector base ~~capacity~~ capacitor . In such a case, the behavior can be improved by providing at diode D1. A high impedance resistor can be connected in parallel to the diode, to provide a DC path when switching-over.

Please replace the paragraph that begins at page 11, line 18 with the following:

According to Fig. 5, instead of a common bias means for the input bipolar transistor and the output bipolar transistor, a respective separate bias means is provided. Thereby, the base of the input bipolar transistor ET is connected to a first bias terminal

Bias2 via a bias resistor Rb3, while the base terminal of the output bipolar transistor AT is connected to a second bias terminal Bias3 via a bias resistor Rb4. To obtain decoupling of the biases provided over the receptive bias terminals Bias2 and Bias3, respectively, the base terminals of the input bipolar transistor ET and the output bipolar transistor AT are DC separated and high frequency-coupled via a coupling ~~capacity~~ capacitor 36. Thus, according to the embodiment shown in Fig. 5, it is possible to set the base potentials of the input bipolar transistor ET and the output bipolar transistor AT separately from on another.